REMARKS

Claims 1, 2, 6, 8-12, 14-16, 19-22, and 24-40 are pending. Claims 1, 2, 6, 8-12, 15, 16, 19-22, and 24 have been amended, claims 3-5, 7, 13, 17, 18, and 23 have been canceled, and new claims 26-40 have been added to recite additional features of the invention.

Reconsideration of the application is respectfully requested for the following reasons.

In the Office Action, claims 1, 3-5, 7-9, 19-21, 24, and 25 were rejected under 35 USC § 102(e) for being anticipated by the Kizer patent. The remaining claims were than rejected under 35 USC § 103(a) based on Kizer taken in combination with one or more of Davis, Lu, Maneatis, Ishikawa, Van der Veer, and Schultz. Claim 1 has been amended to distinguish the invention from all of these references.

Specifically, claim 1 has been amended to recite a measurement circuit to measure duty-cycle distortion in a first clock signal, where the measurement circuit includes (a) a single-input charge pump driven by the first clock signal, (b) a loop filter to output a voltage corresponding to an average of current from the charge pump over a predetermined time, and (c) a bias generator to generate an analog correction signal based on the voltage output from the loop filter. (See, for example, pages 5-7 with reference to Figs. 1, 2, and 3(a)-3(c) for support).

In addition to these features, claim 1 recites a correction circuit to dynamically adjust a delay of at least one edge of a second clock signal based on the analog correction signal received from the bias generator to reduce the duty-cycle distortion in the first clock signal, the first clock signal generated based on the second clock signal. The cited references do not teach or suggest these features, whether taken alone or in combination. (See, for example, pages 5-9, 10, and 11 with reference to Figs. 1, 2, and 3(a)-3(c) for support).

The Kizer patent discloses a system for correcting duty-cycle distortion in a clock signal. As shown in Figure 1A, this system includes a duty cycle corrector 22 that generates a correction signal for input into a duty cycle shaping circuit 14. The duty cycle corrector measures distortion in a clock signal 18 and the shaping circuit corrects the distortion based on the correction signal received from corrector.

The Kizer patent further discloses that the duty cycle corrector is formed from a duty cycle detector 24 which, for example, may be a charge pump. The charge pump outputs current based on the duty cycle of clock signal 18 and an error accumulator 25 determines the duty-cycle distortion based on the output of detector 24.

However, unlike claim 1, the Kizer patent does not disclose "a loop filter to output a voltage corresponding to an average of current from the charge pump over a predetermined time." In the Office Action, the Examiner pointed to Figs. 1A, 1B, and 5A of Kizer, and corresponding portions of its disclosure, for the loop filter feature of the invention. However, these portions of Kizer only disclose an error accumulator for outputting a digital signal which counts the number of errors output from detector 24. Kizer does not disclose a loop filter to output a voltage corresponding to an average of current (an analog signal) from the charge pump over a predetermined time as recited in amended claim 1.

Kizer also fails to disclose "a bias generator to generate an analog correction signal proportional to the duty-cycle distortion in the first clock signal based on the correction voltage output from the loop filter."

Moreover, the Kizer error accumulator 25 generates the control signal which causes shaping circuit 14 to adjust duty-cycle distortion in input clock signal $CLOCK_{VCO}$. However, as mentioned and as shown in Fig. 3, error accumulator 25 is a digital circuit which generates a digital correction signal for input into shaping circuit 14. In contrast, the claimed

invention uses a bias generator to generate an analog correction signal which is proportional to the duty-cycle distortion in the first clock signal and which is based on the correction voltage output from the loop filter. The Kizer patent does not disclose these features.

Finally, claim 1 recites "a correction circuit to dynamically adjust a delay of at least one edge of a second clock signal based on the analog correction signal received from the bias generator to reduce the duty-cycle distortion in the first clock signal, the first clock signal generated based on the second clock signal." Kizer does not disclose a correction circuit of this type.

Because the Kizer patent does not disclose all the features of claim 1, it is respectfully submitted that the Kizer patent cannot anticipate this claim. Applicants further submit that these differences are sufficient to render claim 1 non-obvious and thus patentable over Kizer. Moreover, claims 2, 6, 8, and 9 are submitted to be allowable, not only by virtue of their dependency from claim 1 but also based on the features separately recited therein.

Independent claims 10, 19, and 24 have been amended to recite features similar to those which patentably distinguish claim 1 from the Kizer patent. Applicants respectfully submit that these claims are therefore allowable along with their dependent claims.

The secondary references cited by the Examiner fail to make up for the deficiencies of the Kizer patent.

For example, the Davis patent was cited for its disclosure of reducing duty-cycle distortion to substantially zero. The Davis patent, however, does not teach or suggest the features added by amendment to independent claims 1, 10, 19, and 24. This patent also fails to teach or suggest the features in the dependent claims.

The Lu patent was cited for its disclosure of one period of ICLK. The Lu patent, however, does not teach or suggest the features added by amendment to independent claims

1, 10, 19, and 24. This patent also fails to teach or suggest the features in the dependent claims.

The Maneatis patent was cited for its disclosure of a bias generator which performs duty-cycle correction to 50%. However, the Maneatis circuit does not teach or suggest the features added by amendment to claims 1, 10, 19, and 24, including a correction circuit to dynamically adjust a delay of at least one edge of a second clock signal based on the analog correction signal received from the bias generator to reduce the duty-cycle distortion in the first clock signal, the first clock signal generated based on the second clock signal. Maneatis also omits the coupling of the correction circuit to the detection circuit recited in claim 1. Also, Maneatis is implemented in a delay-locked loop architecture which is a different application from the claimed invention.

Finally, as the Examiner pointed out, the Maneatis circuit performs duty-cycle correction to 50%. However, Maneatis performs this function in a very different way than that claimed, i.e., the invention dynamically adjusts a delay of at least one edge of a second clock signal based on the analog correction signal received from the bias generator to reduce the duty-cycle distortion in the first clock signal, the first clock signal generated based on the second clock signal. In contrast, Maneatis discloses that "Loop1 only uses rising edges in F_{ref} to produce . . . a duty cycle correction of 50%." (Emphasis added). That is, Mineatis does not adjust an edge of an input clock signal but rather adjusts the reference signal which is compared by PFD 612 to an input clock signal. (See Figure 6A).

For the foregoing reasons, it is respectfully requested that the Maneatis patent does not make up for the deficiencies of the Kizer patent, whether taken alone or in combination with the remaining references of record. Applicants further submit that Maneatis fails to teach or suggest the features recited in the amended dependent claims.

The Ishikawa patent was cited for its disclosure of a startup circuit. The Ishikawa patent, however, does not teach or suggest the features added by amendment to independent claims 1, 10, 19, and 24. This patent also fails to teach or suggest the features in the dependent claims.

The Van der Veer patent was cited for its disclosure of achieving a 50 ns response time. The Van der Veer patent, however, does not teach or suggest the features added by amendment to independent claims 1, 10, 19, and 24. This patent also fails to teach or suggest the features in the dependent claims.

The Schultz patent was cited for its disclosure of a global clock network. The Schultz patent, however, does not teach or suggest the features added by amendment to independent claims 1, 10, 19, and 24. This patent also fails to teach or suggest the features in the dependent claims.

New claims 26-40 have been added to the application.

Claim 26 recites that the correction circuit of claim 1 "adjusts a delay of a first edge of the second clock signal based on the analog correction signal from the bias generator and maintains a second edge of the second clock signal at a fixed delay, to reduce the duty-cycle distortion in the first clock signal." These features are not taught or suggested by the references of record, whether taken alone or in combination.

Claims 27-29 recite similar features depending from claims 10, 19, and 24 respectfully. Applicants submit that these claims are also allowable.

Claim 30 recites that "the analog correction signal is indicative of an offset voltage generated by the charge pump current as a result of the duty-cycle distortion in the first clock signal." (See, for example, Figures 3(b)-3(c)). These features are not taught or suggested by the cited references, whether taken alone or in combination.

Claim 31 recites that "the analog correction signal is inversely proportional to the voltage that corresponds to the average current from the charge pump over said predetermined time." (See, for example, page 10 of Applicants' disclosure). These features are not taught or suggested by the cited references, whether taken alone or in combination.

Claim 32 recites that the correction circuit includes a voltage-controlled buffer comprising a buffer circuit and a cascode amplifier coupled to the buffer circuit, the buffer circuit to delay the at least one edge of the second clock signal by an amount controlled a bias voltage generated by the cascode amplifier based on the analog correction signal from the bias generator. (See Figure 5 and corresponding portions of Applicants' specification). These features are not taught or suggested by the cited references, whether taken alone or in combination.

Claim 33 recites that the buffer circuit includes at least one inverter to invert the second clock signal and a plurality of current sources to set a drive strength of the at least one inverter based on the bias voltage from the cascode amplifier. These features are not taught or suggested by the cited references, whether taken alone or in combination.

Claim 34 recites that the current sources set the drive strength by controlling a transition slope of a signal output from the inverter, to thereby adjust high-phase and low-phase portions of the first clock signal. These features are not taught or suggested by the cited references, whether taken alone or in combination.

Claim 35 recites that the bias voltage is inversely proportional to the analog correction signal. These features are not taught or suggested by the cited references, whether taken alone or in combination.

Claim 36 recites that the cascode amplifier includes an active load, a first transistor coupled to the active load, a second transistor connected to the first transistor, and a current-

source transistor coupled to the second transistor and having a gate coupled to receive the analog correction signal, the active load to output the bias voltage for controlling the buffer circuit. These features are not taught or suggested by the cited references, whether taken alone or in combination.

Claim 37 recites that the active load includes a diode-connected transistor. These features are not taught or suggested by the cited references, whether taken alone or in combination.

Claim 38 recites that the diode-connected transistor outputs the bias voltage in inverse proportion to the analog correction signal. These features are not taught or suggested by the cited references, whether taken alone or in combination.

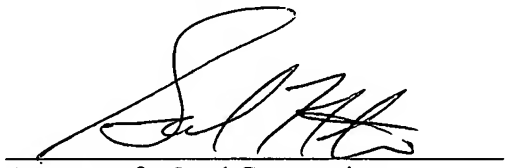
Claim 39 recites that the first and second transistors and the current-source transistor are of a first conductivity and the diode-connected transistor is of a second opposing conductivity. These features are not taught or suggested by the cited references, whether taken alone or in combination.

Claim 40 recites that the first and second transistors and the current-source transistor are maintained in a same state. These features are not taught or suggested by the cited references, whether taken alone or in combination.

In view of the foregoing amendments and remarks, it is respectfully submitted that the application is in condition for allowance. Favorable consideration and prompt allowance of the application is respectfully requested.

To the extent necessary, Applicants petition for an extension of time under 37 CFR § 1.136. Please charge any shortage in fees due in connection with this application to Deposit Account No. 16-0607 and credit any excess fees to the same Deposit Account.

Respectfully submitted,



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